Analysis of Timing Recovery for DMT Systems Over Indoor Power-Line Channels

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Abstract—**Discrete Multitone (DMT) modulation is a suitable technique to cope with main impairments of broadband indoor power-line channels: spectral selectivity and cyclic time variations. To attain higher bit rates, in those subbands with good transmission conditions a high number of bits per symbol must be allocated and, hence, synchronization issues become an important concern. This paper analyzes the performance of a conventional DMT timing recovery scheme designed for linear time-invariant (LTI) channels, like digital subscriber lines, when employed over indoor power-lines. The influence of the channel short-time variations and the sampling jitter on the synchronization scheme performance is assessed. Proper parameterization of the timing recovery scheme is provided on the basis of reducing the impact of channel time variations while maintaining the ability to track the sampling jitter.**

***Index Terms*—indoor power-line, DMT, timing recovery, LPTV channel, cyclostationary noise, jitter.**

I. INTRODUCTION

This work concentrates on the utilization of indoor power grid for broadband data transmission, which in the last years is being pursued by the growing demand for SOHO (Small Office Home Office) networking solutions. In addition to the already well-known characteristics of these channels [1,2], they also present short-term variations whose origin is the dependence of the impedance and the noise generated by the electrical devices connected to the grid on the mains voltage. As a consequence of the time-variant behavior of electrical devices, the channel frequency response exhibits a cyclic short-time variation and the noise presents cyclostationary components [3], both synchronous with the mains.

To cope with the aforementioned impairments, DMT modulation seems to be the most suitable transmission scheme [2]. Its ability to divide the available spectrum in smaller subbands allows to exploit the spectral resources even when they are sparse. Moreover, channel time variations can be overcome by adapting the constellation assigned to each subband.

To make the most of the carriers with high signal-to-noise ratios (SNR), it must be ensured that the received data is sampled at the right instants. To this end, the timing recovery mechanism extracts the sampling information from the received signal and uses it to drive the timing error correction procedure. To accomplish the latter task, an all-digital scheme comprised of a fixed oscillator and a discrete-time domain correction by means of an interpolator filter can be employed [4]. These strategies have been widely studied in digital subscriber line systems [4,5]. However, their performance may be seriously degraded when they are used in an indoor power-line scenario.

This inferior performance has a twofold origin. Firstly, in order to track the short-time variations of the frequency response, the classical frequency equalizer (FEQ) used in DMT must be adapted at a rate comparable to that of the synchronization system, which may cause interaction between them and their eventual divergence [6]. To overcome this pitfall equalization may be performed in two steps, one that compensates for the long-term changes in the channel response and another that follows the short-time variations experienced by the channel with respect to its long-term value. Since the timing recovery scheme must take information from the output of the long-term FEQ, cyclic short-time variations of the channel, with harmonics of 50Hz-60Hz (depending on the mains signal frequency), mislead the estimation of the sampling error. Secondly, when sampling broadband signals (the available bandwidth for power-line systems extends up to 30MHz [7]) the timing scheme must track the short-term instabilities of the sampling period [8], whose influence is usually neglected.

This paper analyses the performance obtained with a conventional synchronization system, designed for DMT systems that operate in LTI channels, when employed over indoor power-line channels. The effects of the channel short-time variations and the sampling jitter are assessed and the parameterization of the timing recovery scheme that minimizes their influence is given. To this end, the system model is firstly described in section II. Afterwards, a detailed description of the timing recovery scheme and simulation results are presented and discussed in section III. Finally, main conclusions drawn from the work are given in section IV.

II. SYSTEM MODEL

A. Channel Model

Indoor power-line channels response can be modeled as a linear periodically time-variant (LPTV) system and an additive cyclostationary noise term. Fortunately, the delay spread of these channels is much smaller than their coherence time, i.e. the channels are *underspread*, and a slow-variation approach can be assumed [3].

Simulations presented in this work have been carried out

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over a set of 24 channels measured in the frequency band from 1MHz to 20MHz in two indoor scenarios: 12 in an apartment of about 80m^2 and 12 in a detached house of about 300m^2. Statistical parameters of these channels can be found in [3]. A representative channel of the ones measured in the apartment has been selected to present qualitative results. In Fig. 1 (a) the frequency response values of the channel in a cycle time in the band from 1MHz to 20MHz have been superimposed (left axis). Fig. 1 (b) shows information about phase changes of the frequency response. However, this time only the peak excursion of the phase along a cycle time, defined as

$$\measuredangle H(f)_{pp} = \max_t \left[\measuredangle H(t,f)\right] - \min_t \left[\measuredangle H(t,f)\right] \qquad (1)$$

where $t \in [0, T_0)$, with $T_0 = 20\text{ms}$, has been depicted (right axis). Noise measured in this channel is shown in Fig. 2, where the values of the instantaneous power spectral density (IPSD) measured along a cycle time have been superimposed.

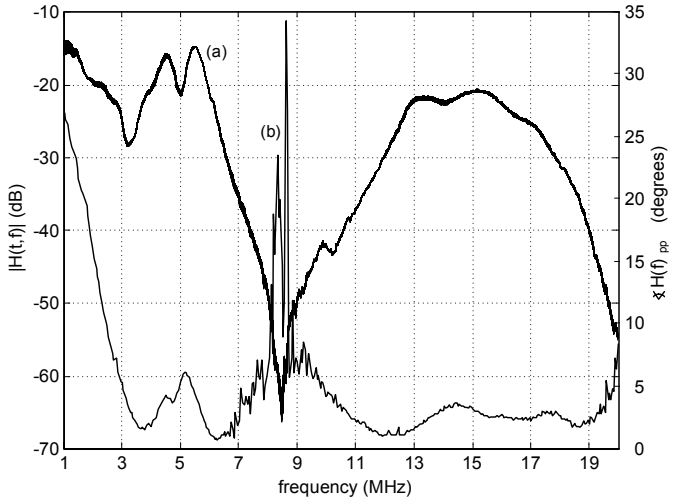

Fig. 1. (a) Superimposed values of the amplitude channel response along the mains cycle. (b) Peak excursion of the channel phase response along the mains cycle.

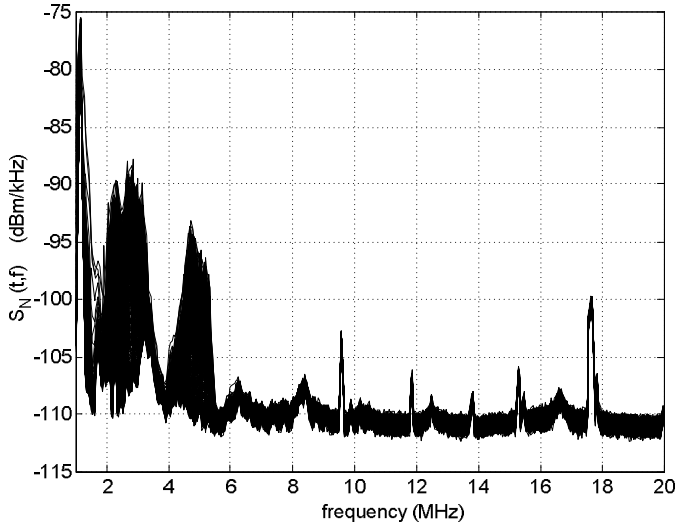

Fig. 2. Superimposed values of the channel noise IPSD along the mains cycle.

Fig. 1 shows that, although there are not significant attenuation changes, remarkable phase changes occur in the 1MHz to 3MHz band and in the vicinity of 5MHz and 9MHz. Concerning the noise ISPD, it is worth noting that differences exceeding 20dB do occur between 2MHz and 3MHz and about 15dB around 5MHz.

Both, the frequency response and the noise IPSD presented in Fig. 1 and Fig. 2 include the effect of a band-pass coupling circuit that serves as an antialiasing filter and protects the receiver from the mains signal.

B. Analog- to-digital conversion model

In the analog-to-digital conversion (ADC) process the sampling instants experience two types of deviation from their nominal values. The first is a systematic effect due to the frequency inaccuracy of the clock that drives the analog-to-digital converter. The influence of this phenomenon in the performance of DMT systems has been widely studied [4,5] and will not be considered in this work unless clearly stated. The second is a random instability with two components: one caused by the random fluctuations of the converter sampling clock period, the so-called oscillator jitter, and another due to the uncertainty in the sampling instant introduced by the sample-and-hold circuit, the so-called aperture jitter [9]. The latter effects have no influence when the sampling frequency is relatively low (as in ADSL), but when the sampling frequency is increased, the relative value of these instabilities in comparison to the sampling period can not be neglected [9].

Random instabilities in a oscillation are caused by a phase noise, $\phi_{osc}(t)$, that has its origin in the noise sources of the circuit that generates the oscillation. Due to the phase noise, the significant instants of the signal, e.g. zero-crossings, experience a time deviation from their nominal values. This is the so-called timing jitter or simply jitter, $\tau_{osc}(t)$, whose relation with the phase noise can be generally approximated by $\tau_{osc}(t) \approx -\phi_{osc}(t)/2\pi f_S$, where f_S is the oscillation frequency.

These instabilities are characterized in the frequency domain by means of the SSB (Single Sideband) Phase Noise Spectrum, defined as [8]

$$\mathcal{L}(f) = 10\log_{10}\left(S_\phi(f)/2\right) \text{ (dBc/Hz)}, \qquad (2)$$

where $S_\phi(f)$ is the PSD of the phase noise and dBc/Hz stands for dB below the carrier in a 1Hz bandwidth.

In the time domain, oscillator phase random fluctuations are characterized by means of the integrated jitter, σ_{osc}, given by

$$\sigma_{osc}^2 = \frac{1}{\left(2\pi f_0\right)^2}\int_{f_L}^{f_H} S_\phi(f)\,df, \qquad (3)$$

where 10Hz and 20MHz are the common values given to f_L and f_H, respectively.

According to the Power-Law model [8], $\mathcal{L}(f)$ can be approximated by a piece-wise linear function whose slopes are in the range from -40dB/decade to 0dB/decade with 10dB/decade steps. Jitter values employed in this work have

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been generated by filtering a gaussian white noise with a cascade of first and second order transfer functions that approximate the different slopes of the phase noise spectrum. Fig. 3 shows the $\mathcal{L}(f)$ curves corresponding to three 100MHz state-of-the-art oscillators with integrated jitter values of 20ps, 10ps and 5ps.

Even if an ideal oscillator could be used, actual sampling instants would fluctuate due to the aperture jitter, $\tau_{adc}(t)$. The aperture jitter is usually modeled in terms of its phase noise PSD, which is assumed to have a Lorentzian shape [11],

$$S_{\phi_{adc}}(f) = 2\pi \frac{\sigma_{adc}^2 f_S^2}{f_S^2/4 + f^2}, \quad (4)$$

where σ_{adc}^2 is the aperture jitter rms value. Fig. 3 depicts the aperture phase noise PSD of a state-of-the-art 12bit, 100MHz sampling frequency analog-to-digital converter with 5ps of rms aperture jitter. As seen, in the frequency band of interest, it is essentially flat.

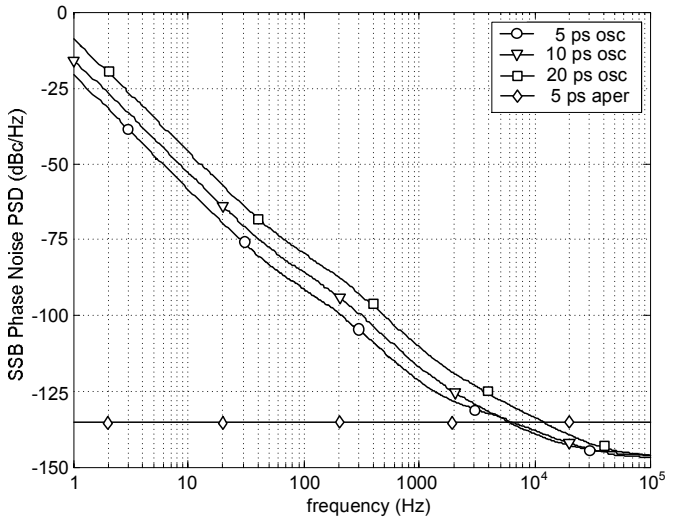

Fig. 3. Oscillator and aperture SSB Phase Noise Spectra.

Since both types of jitter have different origins, their PSD's and integrated jitters values can be summed to obtain the overall jitter contribution that, from now on, will be referred to as ADC jitter.

C. DMT receiver model

The simplified block diagram of an *N* carrier DMT receiver with an all-digital synchronization scheme is shown in Fig. 4. After performing the unsynchronized sampling, timing error correction is carried out in the time domain by means of an interpolator. The FEQ applied after the DFT needs careful design due to the LTPV behavior of the channel. From the statistics of the rate of change of the frequency responses and the Doppler Spread bandwidth shown in [3], it can be concluded that the FEQ taps must be adapted at a rate comparable to that of the synchronization system. In order to avoid interaction between both adaptive systems, two frequency equalization stages are employed. Firstly, a long-term FEQ, *LFEQ*, compensates for the long-term changes in the channel response. Since these changes occur at a rate much slower than the symbol rate, the information needed for timing recovery is taken from the output of this stage. Secondly, a short-term FEQ, *SFEQ*, follows the short-term variations of the channel response with respect to its long-term value. Channels considered in this work do not present long-term changes. Therefore, a fixed *LFEQ* that compensates for the time-average channel over the mains cycle is employed.

The timing recovery scheme follows the conventional digital phase-locked loop (PLL) structure with a phase detector that tries to estimate the phase error due to the unsynchronized sampling and to the ADC jitter, a loop filter and a discrete-time voltage-controlled oscillator (VCO) [6].

III. TIMING RECOVERY SCHEME

A. Description

The input signal is oversampled by a factor of two. The interpolator filter, which also performs the by two decimation, has been designed so that signal distortion is essentially due to the timing recovery mechanism [5].

During data transmission, the phase detector estimates the timing error based on the decided symbols. Pilot-based schemes do not seem to be appropriate due to their larger variance and to the unknown position of the channel frequency response notches.

The maximum likelihood (ML) phase estimator is widely used in DMT systems over LTI wired channels [4]. In these scenarios, assuming that the cyclic prefix length is longer that the channel impulse response, the k-th equalized output of the DFT for the m-th symbol, $Y_{m,k}$, can be approximated (small timing error provided) by

$$Y_{m,k} \approx X_{m,k} e^{j\frac{\pi}{N}k\theta_m} + N_{m,k} FEQ_k, \quad (5)$$

where $X_{m,k}$ denotes the m-th symbol transmitted in carrier k; $N_{m,k}$ is the noise at the k-th output of the DFT performed over the m-th symbol samples; and θ_m is the phase error caused by the uncorrected deviation of the m-th symbol sampling instants with respect to their nominal values. FEQ_k is the k-th tap of a *zero-forcing* FEQ, that in an LTI channel is given by $FEQ_k = H_k^{-1}$, where H_k is the frequency response at the frequency of carrier k. Hence, assuming correct decisions and gaussian noise, the ML estimator of θ_m can be approximated by [4]

$$\widehat{\theta_m} \approx \frac{N}{\pi} \frac{\sum_{k\in K} \left(\mathrm{Im}\left[Y_{m,k} \widehat{X}_{m,k}^* \right] k \Big/ \left(\left| FEQ_k \right|^2 \sigma_{N_k}^2 \right) \right)}{\sum_{k\in K} k^2 SNR_k}, \quad (6)$$

where Im[·] denotes the imaginary part, $\widehat{X}_{m,k}^*$ is the complex conjugate of the detector output, SNR_k is the signal-to-noise ratio experienced by carrier k, K is the set of index carriers

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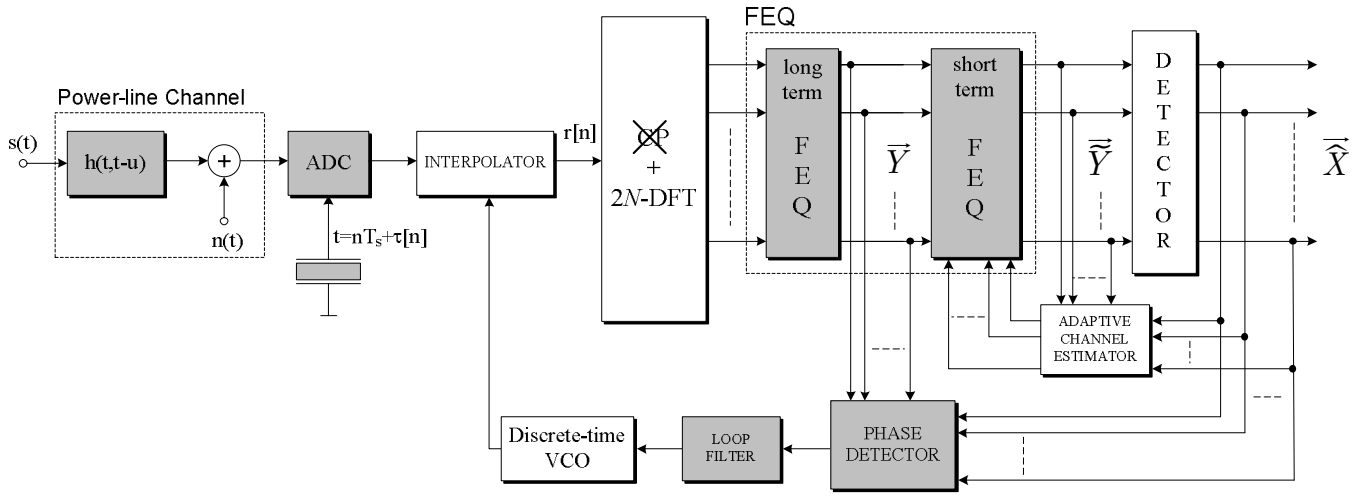

Fig. 4. Simplified block diagram of the DMT receiver.

utilized in the estimation and $\sigma^2_{N_k}$ is the noise power in the band of carrier k.

In order to analyze the output of the ML estimator computed according to (6) in an LPTV channel with cyclostationary noise, it is convenient to express the symbol index, m, in terms of the channel and noise IPSD period. Thus, denoting by T_{DMT} the DMT symbol period and by T_0 the mains signal period, $m = cL + \ell$, with $0 \le \ell \le L-1$ and where $L = T_0/T_{DMT}$. Assuming that the slow-variation approach holds, the output of the *LFEQ* at the frequency of carrier k during the ℓ-th interval of the c-th cycle, $Y^c_{\ell,k}$, can be expressed as

$$Y^c_{\ell,k} \approx X^c_{\ell,k} \left| H_{\ell,k} \right| e^{j\angle H_{\ell,k}} e^{j\frac{\pi}{N}k\theta^c_\ell} LFEQ_k + N^c_{\ell,k} LFEQ_k , \qquad (7)$$

where $H_{\ell,k}$ denotes the frequency response of the channel at the frequency of carrier k during the ℓ-th interval and $N^c_{\ell,k}$ is the noise value at the output of the DFT at the frequency of carrier k during the ℓ-th interval of the c-th cycle.

Since the *LFEQ* only compensates for the time-averaged value of the frequency response, $LFEQ_k = \langle H_{\ell,k} \rangle^{-1}$, where $\langle \cdot \rangle$ denotes averaging over the variable ℓ, the output of the phase detector in (6) would be misled by the short-time cyclic changes of the channel.

The output of the phase detector is fed to the loop filter, whose transfer function,

$$L(z) = \alpha + \frac{\beta}{1 - z^{-1}}, \qquad (8)$$

is selected so that a second order type II PLL [6] results.

B. Performance

This subsection analyzes the performance of the above synchronization scheme when employed over the 24 actual channels characterized in [3]. The channel presented in Fig. 1 and Fig. 2 has been selected to present qualitative results. Throughout the work a DMT system with $N = 512$ carriers distributed in the frequency band up to 25MHz is employed. Nevertheless, only carriers with indexes $22 \le k \le 409$, i.e. in the band from approximately 1MHz to 20MHz, are finally used. The ADC is carried out with a sampling frequency of $1/T_s = 100$MHz. The cyclic prefix length, *cp*, has been fixed to 226 samples at $1/(2T_s)$, which ensures that the power of ISI and ICI due to the spectral distortion of the channel will be much lower than the channel noise level. This *cp* length also makes T_0/T_{DMT} an integer value, which simplifies the subsequent performance analysis. An ideal equalization is performed, i.e. the *LFEQ* and *SFEQ* are provided with precise values of the actual frequency response. The output of the transmitter is launched into the channel with a PSD of -20dBm/KHz. All carriers whose symbol error probability for a BPSK constellation is less or equal than 10^{-5} at all time intervals, ℓ, are employed for data transmission and phase estimation. The loop filter is configured for the overall PLL response to be critically dumped.

Fig. 5 shows the output of the loop filter when the only non-ideal effect introduced by the ADC is a frequency offset of 20ppm. The equivalent noise bandwidth of the loop is set to 510Hz.

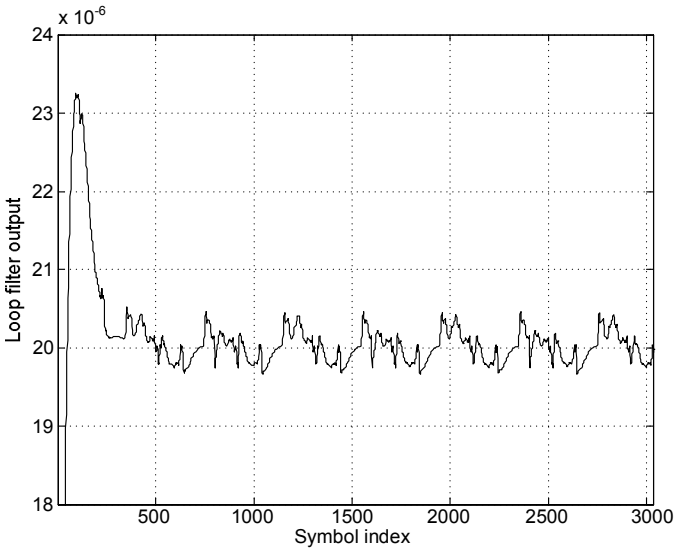

Fig. 5. Loop filter output in the channel of Fig. 1 and Fig. 2 for a frequency error of 20ppm.

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The amplitude of the periodical components observed in Fig. 5, caused by the LPTV nature of the channel, can be diminished by reducing the loop bandwidth. However, this leads to longer convergence times and, therefore, to a reduction in the capacity of the loop to follow timing fluctuations like the ones shown in Fig. 3. Surprisingly, this reduced capacity is not primarily due to the power of the jitter filtered out by the loop [10], which is mainly concentrated in very low frequencies. Indeed, for small but practical loop bandwidths, i.e. implementable in fixed-point arithmetic and with reasonable convergence times, low frequencies are amplified by the loop due to the unavoidable peaking that appears in the frequency response of a critically dumped second order type II PLL [6].

Performance of the timing recovery procedure is firstly characterized in terms of the signal-to-distortion ratio (SDR) at the detector input, which for small timing errors can be approximated by

$$SDR_k = \frac{1}{M}\sum_{m=1}^{M-1}\frac{1}{\left|1-e^{j\frac{\pi}{N}k\theta_m}\right|^2}, \qquad (9)$$

where M is the number of symbols received during transmission phase and θ_m is the phase error caused by the uncorrected timing errors experienced by the m-th symbol. Fig. 6 shows the SDR values experienced by the last used carrier ($k=409$) as a function of the loop bandwidth for the ADC jitters shown in Fig. 3. Although curves are labeled according to the oscillator integrated jitter values, a 5ps aperture jitter is also included in all cases. Two additional curves have been depicted to highlight the individual effect of channel cyclic variations and ADC jitter in the system performance. One of them shows the SDR values obtained when the 20ps oscillator is employed in a LTI channel whose frequency response is equal to the time-average value of the one presented in Fig. 1. The other depicts the SDR values obtained when the time-variant channel shown in Fig. 1 and Fig. 2 is employed and no jitter is introduced in the ADC process.

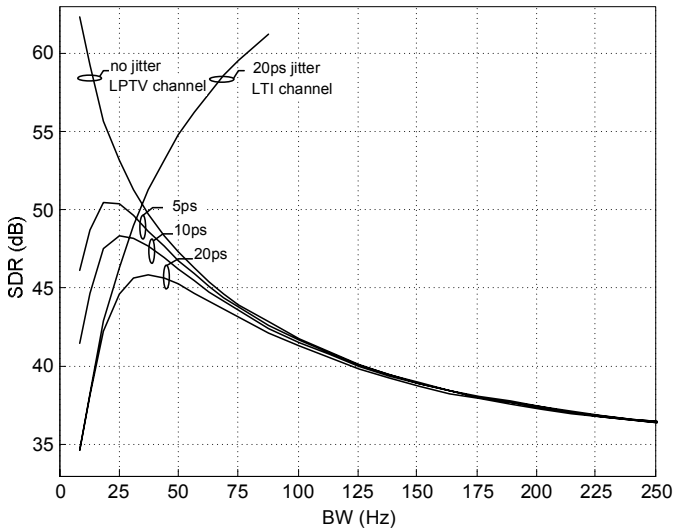

Fig. 6. SDR values in the last used carrier in different situations.

Curves in Fig. 6 illustrate the clear trade-off between attenuation of the channel response cyclic variations in the phase error estimates and loop's ability to follow the ADC jitter. For larger loop bandwidths the SDR is low because phase error estimates are strongly misled by the cyclic short-time variation of the frequency response (the cyclostationary noise has much less influence). As the loop bandwidth is reduced, the SDR increases because channel time variations are attenuated. This process continues until the inability of the loop to follow the ADC jitter becomes the dominating factor in the signal distortion. It is worth noting that performance degrades fast in this zone.

The ultimate system performance parameter is the achievable bit-rate. Its exact computation can be accomplished by approximating the signal at the detector input by

$$\widetilde{Y}^c_{\ell,k} \approx X^c_{\ell,k}e^{j\frac{\pi}{N}k\tilde{\theta}^c_\ell} + N^c_{\ell,k}H^{-1}_{\ell,k}, \qquad (10)$$

where $\tilde{\theta}^c_\ell$ is the uncorrected phase error remaining after the frequency equalization and is comprised of the sum of a periodical component caused by the channel variation and a random gaussian term due to the jitter [10]. However, values calculated in this way may not reflect the bit-rate attained by an actual system. A practical procedure to determine the bit load of each carrier in a real receiver would estimate the signal-to-noise-and-distortion ratio (SNDR) and, according to the usual assumption of an additive gaussian noise and distortion (quite accurate for the ISI and ICI) would calculate the bit load for each carrier by means of a predefined look-up table. Fig. 7 depicts the bit-rate values obtained with this procedure in the channel shown in Fig. 1 and Fig. 2. Two different system working principles have been considered. In the first one, an adaptive modulation strategy is used to make the most of the time-varying channel conditions. In the second, the same constellation is employed throughout the cycle. BPSK and QAM constellations subject to an instantaneous symbol error probability criterion of P_e=10^{-5} and a maximum of 16 bits/symbol have been utilized in both cases.

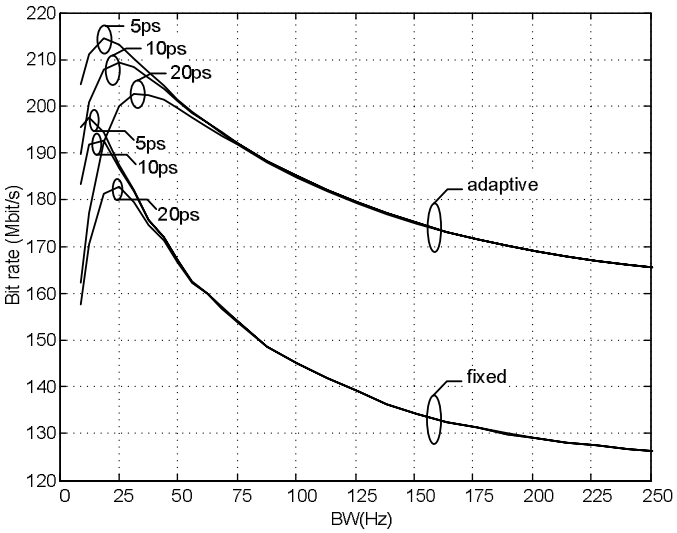

Fig. 7. Bit-rates estimated from SNDR values and a look-up table.

It can be observed that differences between the bit-rates shown in Fig. 7 experience a considerably increment when the loop bandwidth is enlarged. For instance, when the 5ps case is

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considered, the bit-rate gain obtained with the adaptive system is about 8.5%. When a 160Hz bandwidth is employed, this gain goes up to about 30%. This effect is a consequence of the increased dispersion in the SDR values caused by the higher influence of the channel time variations at the output of the phase detector when larger bandwidths are used. Fig. 7 also shows the great sensitivity of the bit-rate with respect to the bandwidth, especially in the region where it is limited by the jitter. Thus, a 10Hz bandwidth reduction over the optimum values for the 5ps case reduces the performance of both, the adaptive and the non-adaptive systems, to nearly the ones of the 20ps case. Hence, the investment in a better oscillator is not always productive.

Once the qualitative effects of jitter and short-time variations in the timing recovery mechanism have been presented, statistical values of the performance degradation computed over the 24 channels referred in section II are now given. Table I shows the bit-rate loss experienced in both scenarios for each oscillator and modulation strategy (adaptive and fixed) when the loop bandwidth is fixed to the average value (computed over the optimum bandwidth values of the 24 channels, which are in the range from 10Hz to 30Hz). Bit-rates obtained in each channel under perfect synchronization conditions are taken as reference for the percentage calculation. As seen, performance degradation due to the synchronization system is smaller in the detached house scenario. This is due to the inherently worse characteristics of these channels, which are established over longer and more branched links than in the apartment. In this latter scenario, signal distortion caused by the synchronization system may cause considerable performance loss, especially when a fixed modulation scheme is employed.

Values in Table I represent the minimum bit-rate loss attainable with the conventional timing recovery scheme. As shown in Fig. 7, an error of just a few tens of Hz in the selection of the loop bandwidth may result in much greater performance degradations.

TABLE I
AVERAGE BIT-RATE LOSS (%) IN EACH SCENARIO WHEN THE MEAN LOOP BANDWIDTH VALUE IS EMPLOYED IN ALL THE CHANNELS

Scenario	σ_{osc}=20ps	σ_{osc}=10ps	σ_{osc}=5ps
Apartment (adaptive)	8.9	6.5	4.6
Apartment (fixed)	14.8	12.4	12.2
Detached-house (adaptive)	2	1.3	0.8
Detached-house (fixed)	3.7	2.8	2.7

IV. CONCLUSION

In this paper, the performance of a conventional DMT timing recovery scheme designed for LTI channels have been assessed in indoor-power line channels. Frequency equalization procedure is accomplished in two steps to avoid the interaction that would occur between a one-step fast adaptive FEQ, needed to track short-time variations, and the synchronization system.

It is shown that performance is limited by two causes: the periodical components induced by the cyclic channel time variations in the phase error estimator and the ability of the timing loop to track the jitter introduced in the analog-to-digital conversion process, which have been shown to be of particular importance in this case. When the loop bandwidth is reduced, channel time variations in the timing error estimates are attenuated, but the capacity of the loop to follow the jitter decreases. The optimum loop bandwidth, which is in the range from 10Hz to 30Hz, results from the trade-off between these effects.

Approximated bit-rate values are given for the situation in which the system employs an adaptive modulation strategy and for the case in which the same constellations are used throughout the cycle. It is shown that in the working zone in which performance of the timing scheme is limited by the jitter, both systems are nearly equally sensitive to loop bandwidth values. However, in the working zone limited by channel time variations, the adaptive system is much less affected by the distortion caused by the timing recovery mechanism.

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